Analog Reinvented

SABRE9602C
SABRE Headphone Driver with Output Switch

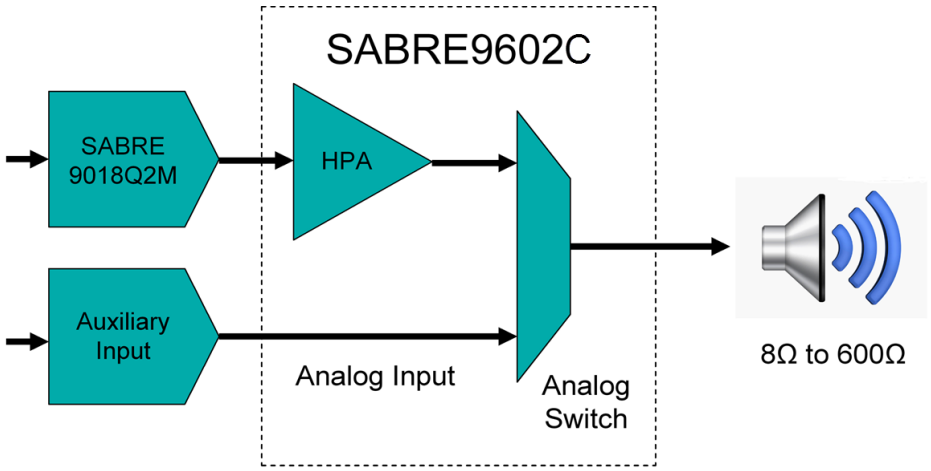
The ***SABRE9602C Headphone Driver and Output Switch*** is the industry's highest performance, standalone headphone driver targeted for audiophile-grade portable applications such as mobile phones, tablets and digital music players.

The ***SABRE9602C Headphone Driver and Switch*** delivers 122dB SNR and –123dB THD, a new benchmark in standalone headphone driver performance that will satisfy the most demanding audio enthusiasts.

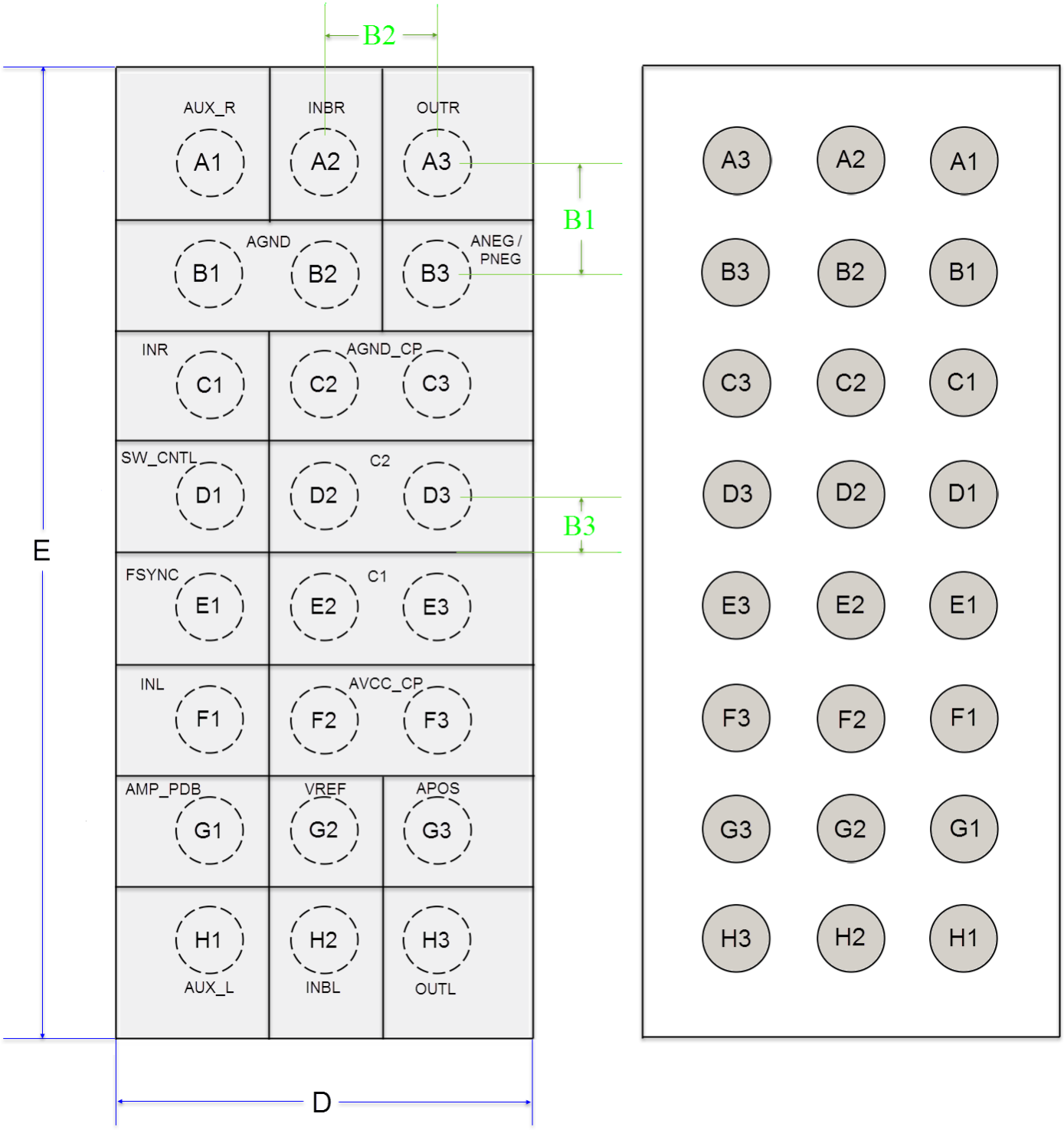
The ***SABRE9602C Headphone Driver and Switch*** is available in a 24-Ball Chip Scale Package (CSP)

Like ESS' high-quality SABRE[32] Reference DACs, the ***SABRE9602C Headphone Driver and Switch*** sets the standard for HD Audio performance with **SABRE SOUND™** quality for today's most demanding audio applications.

FEATURE	DESCRIPTION
Unmatched performance ○ +122dB SNR ○ –123dB THD, 2Vrms into 100kΩ load ○ –117dB THD+N, 2Vrms into 600Ω load ○ –102dB THD+N, Pout = 49mW into 32Ω load	○ Industry's highest performance audio headphone or line-out driver for mobile applications ○ Delivers SABRE SOUND™ quality all the way to the headphones
Ground-referenced output	○ Eliminates large blocking capacitors
Pop-noise suppression	○ Powers up and down without any clicks or pops
Charge pump for negative supply	○ Single AVCC operation simplifies power supply
24-Ball CSP	○ Minimizes PCB footprint
7mA / < 5μA, quiescent / standby current	○ Maximizes battery life



PIN LAYOUT



Top-Through View (Bumps Down) **Bottom View (Bumps Up)**

Detailed Package Dimensions on page 17

PIN DESCRIPTIONS

Pin	Name	I/O	Description
A1	AUX_R	I	Auxiliary Analog Input to the Headphone Switch (Right Channel)
A2	INBR	I	Differential Negative Analog Input (Right Channel)
A3	OUTR	O	Headphone Amplifier Right Channel Output
B1 & B2	AGND	Ground	Analog Ground
B3	ANEG & PNEG	Power	Negative Charge Pump Output and Amplifier Supply Input. Connect a 22µF minimum decoupling capacitor from B3 to ground. Increasing the hold capacitor value will improve supply regulation but increases start-up time.
C1	INR	I	Differential Positive Analog Input (Right Channel)
C2 & C3	AGND_CP	Ground	Analog Ground for the Charge Pump
D1	SW_CNTL	I	Control Input for the Headphone Output Switch. Active-low for HPA signal.
D2 & D3	C2	–	Negative Flying Capacitor connection. Link D2 and D3 together and connect a 4.7µF, low-ESR capacitor between D2/D3 and E2/E3
E1	FSYNC	I/O	Oscillator drive signal. Pin can be used to synchronize multiple devices together with the same charge-pump frequency. Charge pump internal frequency is typically 120kHz with a 0-3.3V amplitude.
E2 & E3	C1	–	Positive Flying Capacitor connection. Link E2 and E3 together and connect a 4.7µF, low-ESR capacitor between E2/E3 and D2/D3
F1	INL	I	Differential Positive Analog Input (Left Channel)
F2 & F3	AVCC_CP	Power	Analog Power for the Charge Pump
G1	AMP_PDB	I	Active-low Power Down (High for normal operation)
G2	VREF	–	Reference Voltage. A 4.7µF X7R dielectric, ceramic capacitor must be connected between VREF and AGND, see Figure 2. The capacitor controls power up and power down of the AUX input switch and the value specified ensures click-less operation
G3	APOS	Power	Positive Supply for Headphone Amplifiers. Decouple with a 22µF minimum, low-ESR ceramic capacitor to ground
H1	AUX_L	I	Auxiliary Analog Input to the Headphone Switch (Left Channel)
H2	INBL	I	Differential Negative Analog Input (Left Channel)
H3	OUTL	O	Analog Left Channel Output

FUNCTIONAL DESCRIPTION

The SABRE9602C has a pair of CMOS FET input amplifiers that exhibit a total A-weighted SNR of better than 122dB when driving 2Vrms into a 600Ω load. The SABRE9602C has an open-loop gain well in excess of 120dB which together with the input stage's excellent linearity is the key to its unparalleled –123dB distortion performance. Please note that the amplifier distortion performance far exceeds that of typical external passive components. Therefore, to achieve the THD performance specified for the SABRE9602C, ensure that the external resistors have a very low, voltage coefficient of resistance, e.g. thin film resistors. Tight tolerance ±0.1% thin-film resistors are recommended for all gain-defining components.

Charge Pump

The SABRE9602C features a low-noise charge pump. The 120kHz switching frequency is above the audio band and, thus, does not interfere with audio signals. The switches are controlled by turn-on and turn-off transistors that operate in a particular sequence that minimizes pops and clicks. The IC requires a 4.7μF minimum flying capacitor between pins E2/E3 and D2/D3 and a 22μF minimum hold capacitor from ANEG/PNEG to AGND_CP. The chip's FSYNC pin offers three connection options: capacitance may be added from FSYNC to ground to slow down the oscillator (100kHz minimum), a logic signal can drive the FSYNC pin to set a fixed frequency, or the FSYNC pins of several SABRE9602C chips may be connected together to force them to run synchronously. When driving the FSYNC pin from an external oscillator, the frequency should be in the range 450kHz to 2.5MHz. The charge pump's internal switching rate is actually at FSYNC/4 so it is easy to interfere with the audio band with only modest changes in the FSYNC frequency.

Charge-Pump Capacitor Selection

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. For best performance over the extended temperature range select capacitors with a minimum X5R dielectric, the X7R dielectric is preferred. The charge pump can be disabled by grounding FSYNC which reduces quiescent current from the +3.3V supply. Disabling the charge pump is recommended when using an external –3.3V supply connected to ANEG.

Flying Capacitor (C4, see Figure 2)

The value of the flying capacitor (C4, connected across pins C1 and C2) affects the charge pump's load regulation and output resistance. A capacitance value (C4) that is too small reduces the current drive capability, which leads to a loss of output voltage. Increasing the value of C4 improves load regulation and reduces the charge-pump output resistance to an extent. With a 4.7μF flying capacitor, the on-resistance of the switches dominates. Use a low-ESR ceramic or electrolytic capacitor for C4. If an electrolytic capacitor is used the correct polarity must be observed, see Figure 2. The flying capacitor C4 can be eliminated when an external –3.3V supply is used & the internal oscillator is disabled by grounding the FSYNC pin.

Hold Capacitor (C2, see Figure 2)

The value of the hold capacitor C2 (connected between ANEG/PNEG and ground) and its Equivalent Series Resistance (ESR) directly affects the ripple voltage at PNEG. Use a low-ESR 22μF minimum capacitor for C2 and also choose the correct voltage rating. C2 can be a ceramic or electrolytic capacitor, if an electrolytic capacitor is used, the correct polarity must be observed, see Figure 2. Increasing the value of the hold capacitor will improve regulation but will increase start-up time.

Amplifier Gain

The recommended gain setting for SABRE9602C is 0dB (Unity Gain). The feedback resistors R2 and R10 of Figure 2 should match the output impedance of the DAC or other signal source. For example, when working with the ES901xK2M, only the feedback resistors, R2 and R10, are required. The recommend value in this configuration is 806Ω which gives the best DNR.

Compensation Components (see Figure 2)

For optimum performance, the following capacitors should be included in all configurations of the SABRE9602C. C1 and C6 control the bandwidth of the SABRE9602C, along with the matching networks C3 and C5. These compensation capacitors should have a low temperature coefficient of capacitance, NP0/C0G types are highly recommended.

Driving a Low-Impedance Load

In order to drive a load of 32Ω or less it may be necessary to use an external –3.3V supply depending on the load's power requirements. When using an eternal negative supply, it is advisable to disable the internal charge pump by connecting FSYNC (pin E1) to analog ground. ANEG/PNEG (pin B3) is connected to an external –3.3V supply and decoupled with a 22μF (minimum) capacitor to AGND_CP. Please check the polarity on the decoupling capacitor C2, see Figure 2. To prevent clicks/pops at startup and shutdown the +3.3V and –3.3V supplies should be sequenced. The +3.3V must be ON and stay ON before connecting or disconnecting the –3.3V external supply.

Short-Circuit Protection (see Figure 2)

To protect the SABRE9602Q under short-circuit conditions 4.7Ω resistors should be placed in series with each output, OUTL and OUTR, but the resistors should be inside the feedback loop.

Output Switch

The headphone output is selected by an ultra-low THD analog switch that connects either to the HD audio headphone amplifier or to an alternate audio source (inputs AUX_L and AUX_R). The auxiliary input may be a voice or lo-fi music signal in a cell phone application. The ultra-low ON-resistance analog switch introduces minimal THD whether it's set to the built-in SABRE headphone amplifier or the alternate source. The switch control input SW_CNTL (pin D1) is active-low, connecting the headphone amplifier to the headphones when grounded. The auxiliary inputs are enabled when the SW_CNTL input is high and the headphone amplifier is shut down by pulling the AMP_PDB (pin G1) low. If the AMP_PDB pin is high, the SW_CNTL pin has no affect. A capacitor, C7 in Figure 2, connected between VREF (pin G2) and AGND controls the power up and power down of the output switch. The value specified for C7 ensures click-less operation of the switch.

SABRE9602C Block Diagram

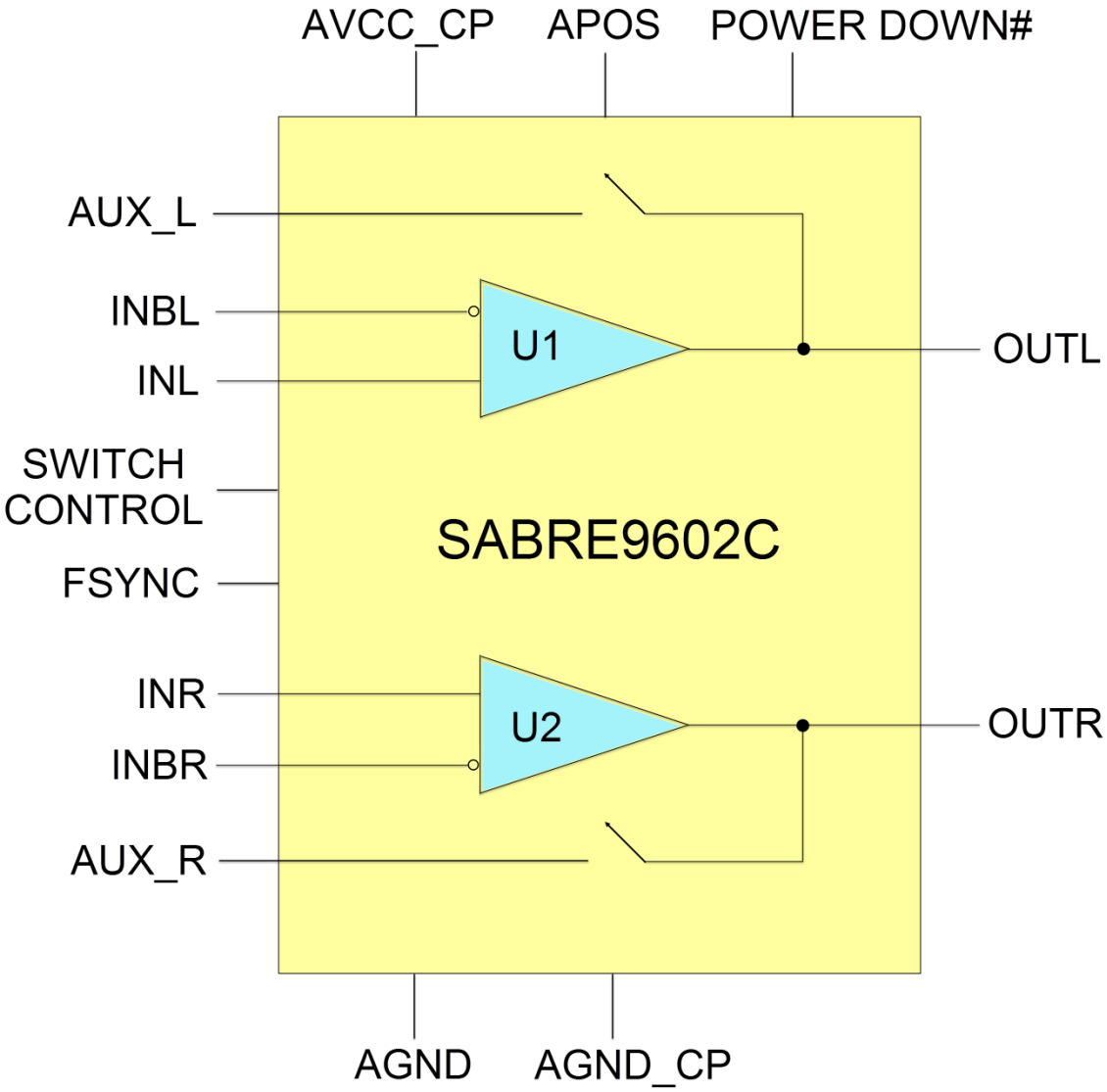


Figure 1. Block Diagram of the SABRE9602C.

APPLICATION DIAGRAM

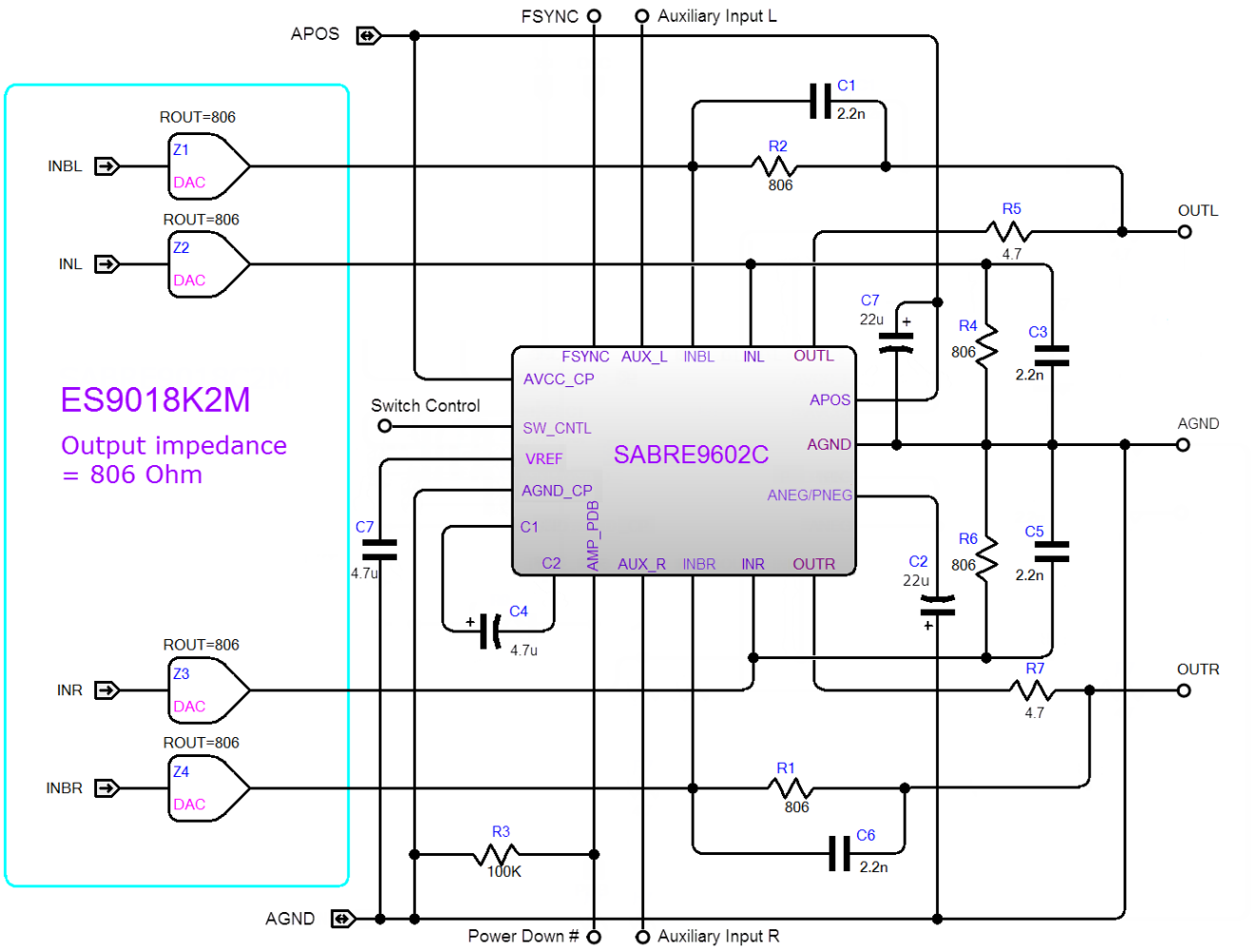


Figure 2. Simplified SABRE9602C Application Circuit.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Storage temperature	–65°C to +105°C
Voltage range for digital input pins	–0.3V to AVCC+ 0.3V
ESD Protection Human Body Model (HBM) Machine Model (MM) Charge Device Model (CDM)	 2000V 200V 500V

WARNING: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS
Operating Temperature	T_A	–20°C to +70°C

Power Supply	Symbol	Voltage	Quiescent Current (Note 1)	Standby Current (Note 2)
Power supply voltage	AVCC_CP APOS	+3.3V ± 5%	7mA typical	300µA typical
Analog power supply voltage (Headphone amplifier disabled)	AVCC_CP APOS	+3.3V ± 5%	300µA typical (AUX input enabled)	< 5µA (AUX input disabled)

Power Supply	Symbol	Load Resistance	Supply Current (Note 3)	Output Voltage (Note 4)
Power Supply current at +3.3V	I_{SY}	32Ω	50mA typical	800mVrms @ 1kHz

Notes

1) Input idling, output unloaded, internal oscillator, all external supply voltages at nominal center values
2) AMP_PDB held low, AUX inputs active
3) Supply current is with both outputs loaded and driven at 800mVrms
4) 800mVrms sine wave across 32Ω load produces a 20mW output

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Minimum	Maximum	Unit
VIH	High-level input voltage	1.4		V
VIL	Low-level input voltage		0.4	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Bias Current	I_B	INL, INBL, INR, INBR inputs	–1.0	0.1	+1.0	nA
Output Offset Voltage	V_{OS}	OUTL to AGND & OUTR to AGND, no input signal	–2.0	0.1	+2.0	mV

ANALOG PERFORMANCE

Test Conditions (unless otherwise stated)

T_A = 25ºC, APOS = AVCC_CP = +3.3V, 1kHz signal, C2 = 22µF, C4 = 4.7µF, FSYNC = open (Figure 2 configuration)

1. SNR / DNR: A-weighted over 20Hz-20kHz in averaging mode
2. THD+N: un-weighted over 20Hz-20kHz bandwidth

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Signal-to-Noise Ratio	SNR	VOUT = 2.0Vrms, A-weighted, RL = 600Ω		122		dB
Total Harmonic Distortion	THD	VOUT = 2.0Vrms, RL = 100kΩ		–123		
Total Harmonic Distortion plus Noise	THD+N	VOUT = 2.0Vrms, RL = 600Ω		–117		dB
		POUT = 49mW into 32Ω		–102		dB
External FSYNC range	FSYNC	FSYNC pin is driven by an external oscillator	450		2500	kHz
Power Supply Rejection	PSR	fin = 217Hz, 200mVp-p ripple		–89		dB
		fin = 1kHz, 200mVp-p ripple		–89		dB
		fin = 10kHz, 200mVp-p ripple		–82		dB
AUXILIARY ANALOG INPUTS						
Input Voltage		Ground referenced			1.0	Vrms

Test Conditions (unless otherwise stated)

T_A = 25ºC, APOS = +3.3V, 1kHz signal, C2 = 22µF, C4 = 4.7µF, FSYNC = 0V, ANEG / PNEG = –3.3V external supply

1. SNR / DNR: A-weighted over 20Hz-20kHz in averaging mode
2. THD+N: un-weighted over 20Hz-20kHz bandwidth

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Signal-to-Noise Ratio	SNR	VOUT = 2.0Vrms, A-weighted, RL = 600Ω		122		dB
Total Harmonic Distortion plus Noise	THD+N	POUT = 49mW into 32Ω load		–102		dB
		1.3Vrms into 16Ω		–106		dB
		1.0Vrms into 8Ω		–102		dB

TYPICAL PERFORMANCE CURVES

The following typical performance curves are generated using ESS' evaluation board as shown in Figure 12. The internal charge pump is used to supply the negative rail. Measurements are taken using an Audio Precision Audio Analyzer. Note that all measurements in the graphs include errors due to the test equipment plus those of the ES9018K2M DAC on the evaluation board. Although these errors are very low, they are significant when measuring a state-of-the-art headphone amplifier like the SABRE9602C. Therefore the parametric values shown in the characteristic curves are slightly degraded compared to the values in the tables as the latter are calculated from measurements in near-ideal conditions.

TYPICAL PERFORMANCE CURVES

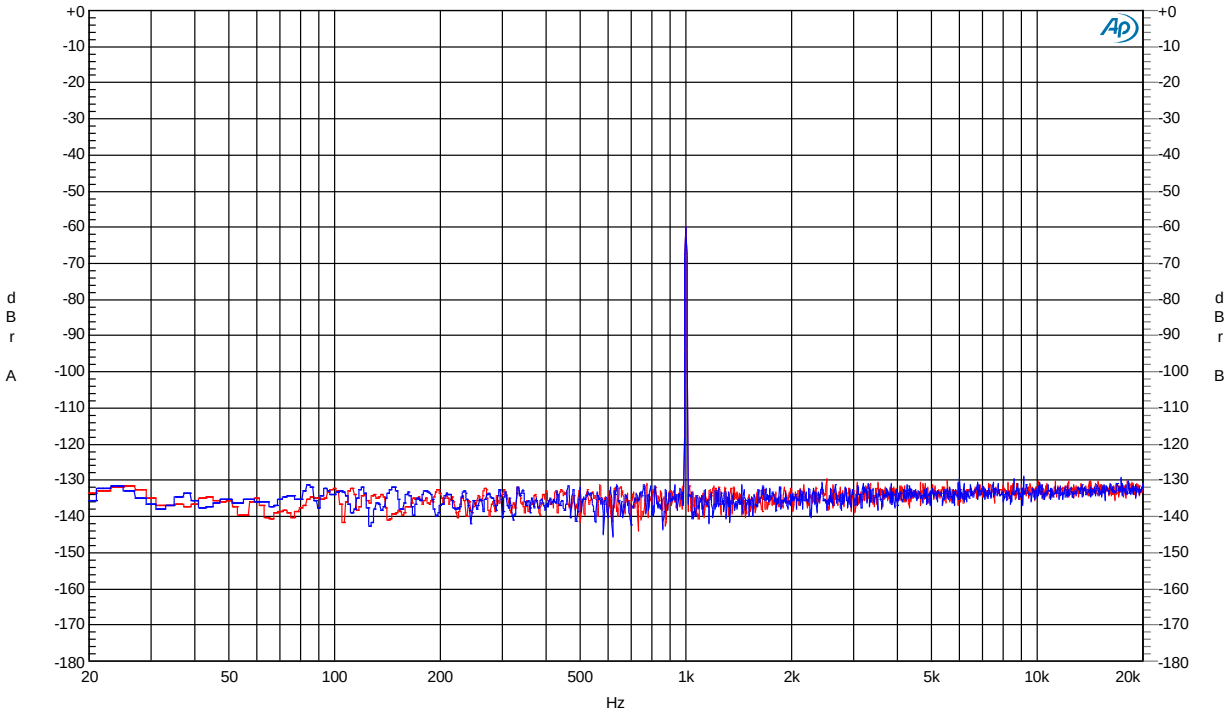


Figure 3. DNR FFT, 1kHz @ –60dB, Single-Ended, 32Ω Load

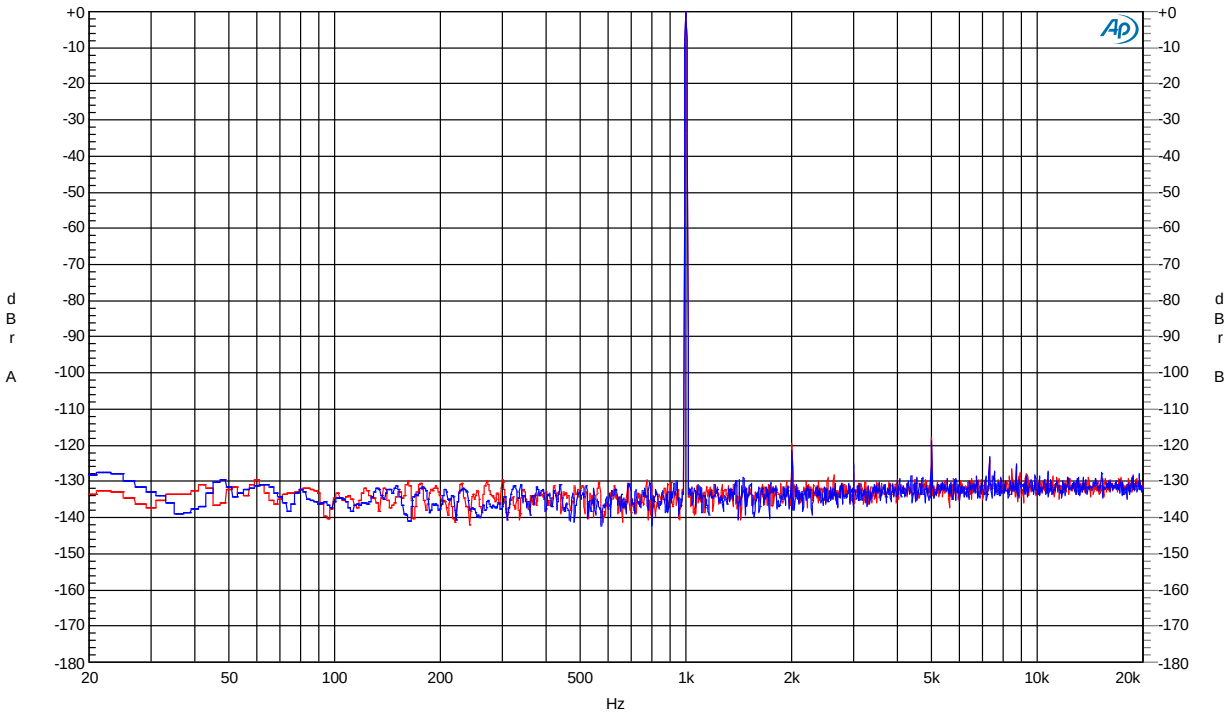


Figure 4. THD+N FFT, 1kHz @ –6dB, Single-Ended, 32Ω Load

TYPICAL PERFORMANCE CURVES

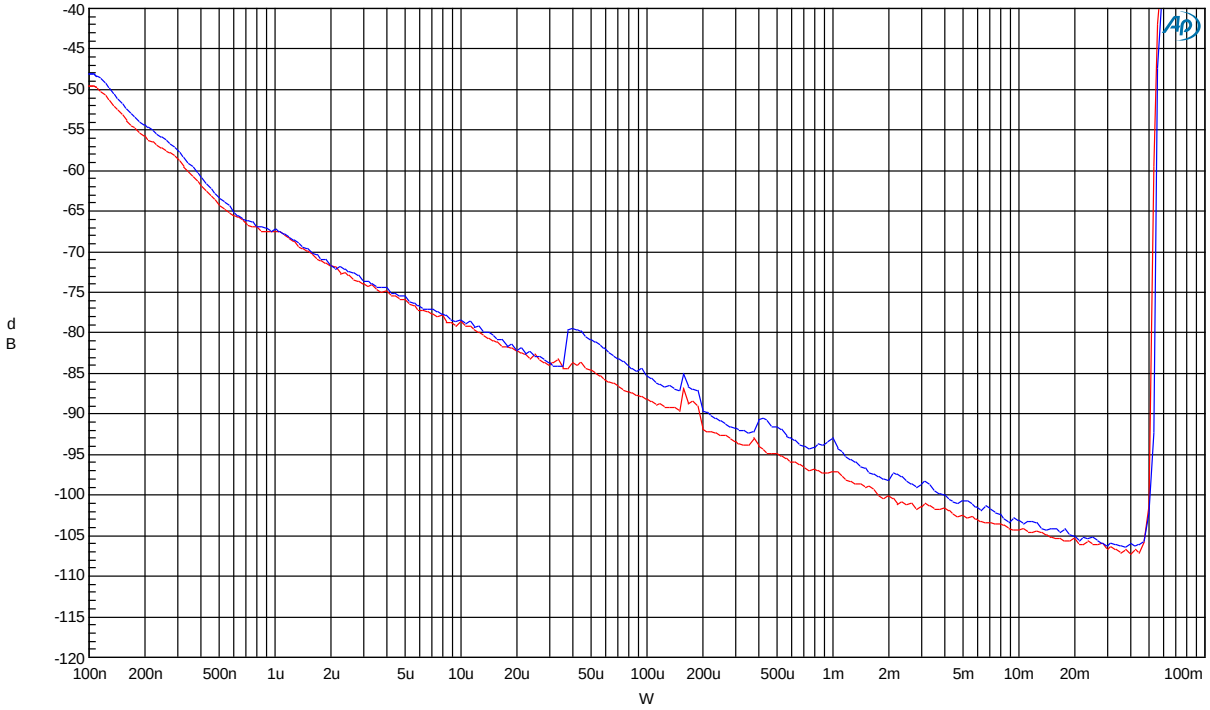


Figure 5. THD+N Unweighted vs. Output Power, Dual Channel Drive, Single Ended, 32Ω Load

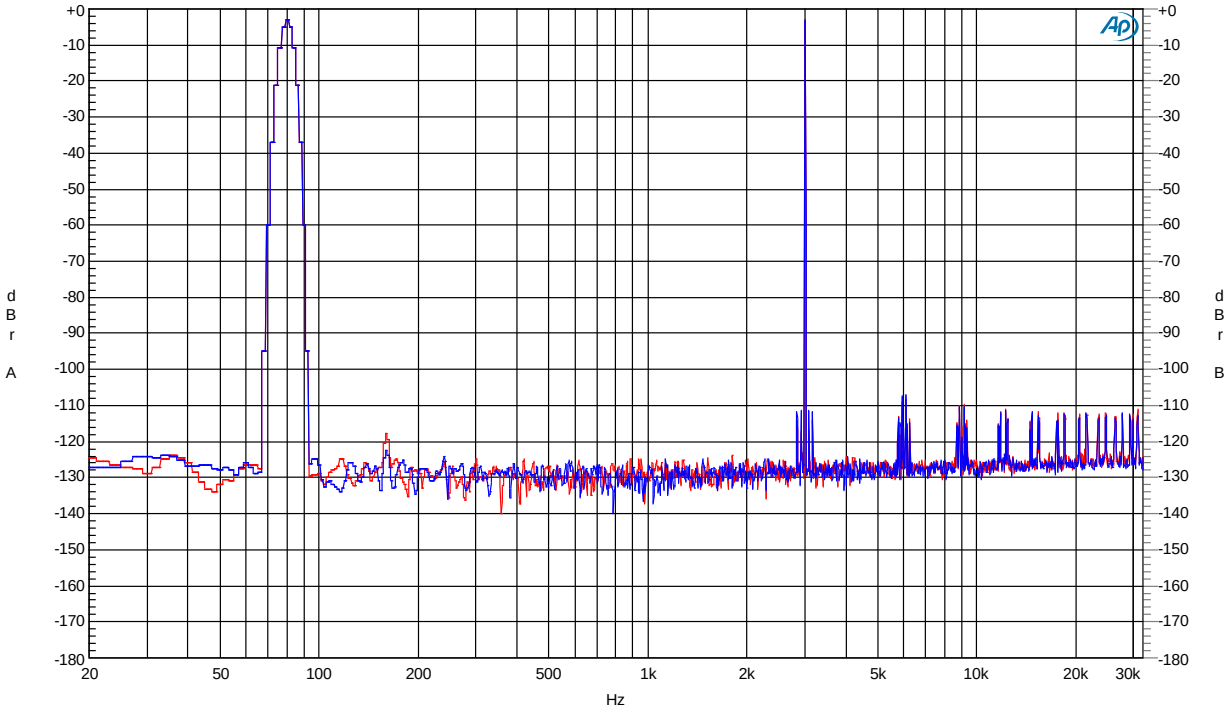


Figure 6. IMD FFT, 3kHz & 80Hz @ SMPTE 1:1, Single Ended, 32Ω Load

TYPICAL PERFORMANCE CURVES

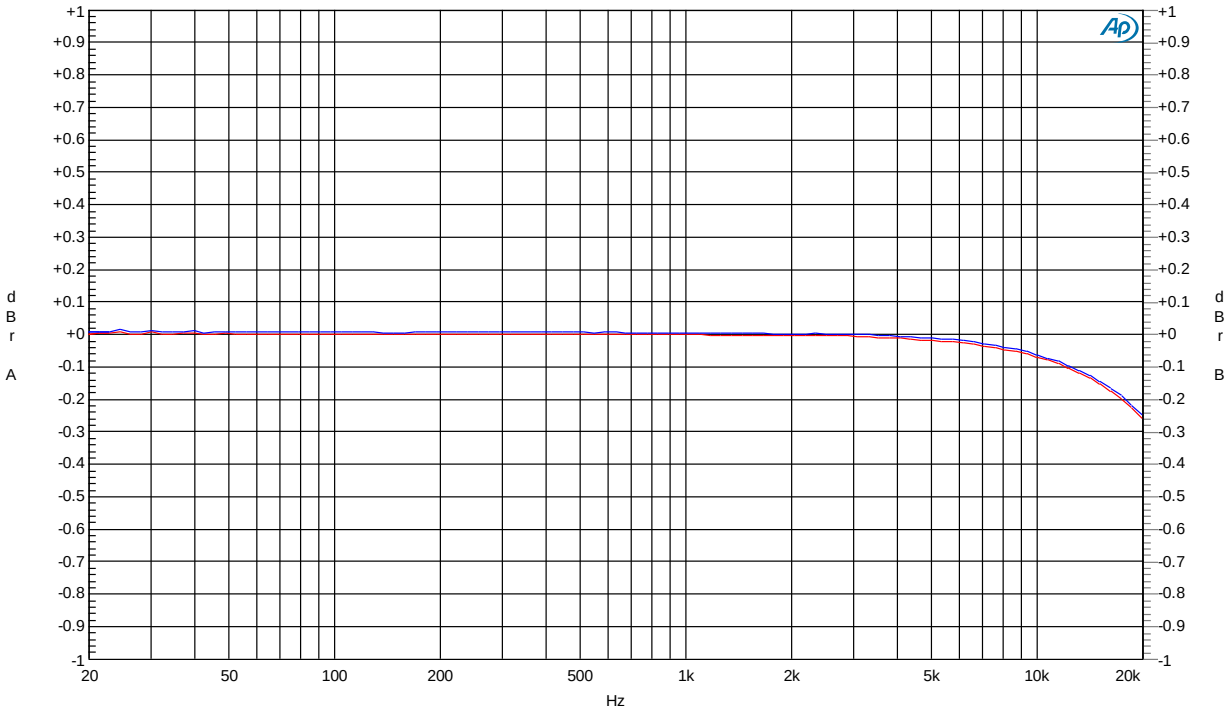


Figure 7. Frequency Response, 20Hz to 22kHz @ 0dB, Log Scale, Single Ended, 32Ω Load

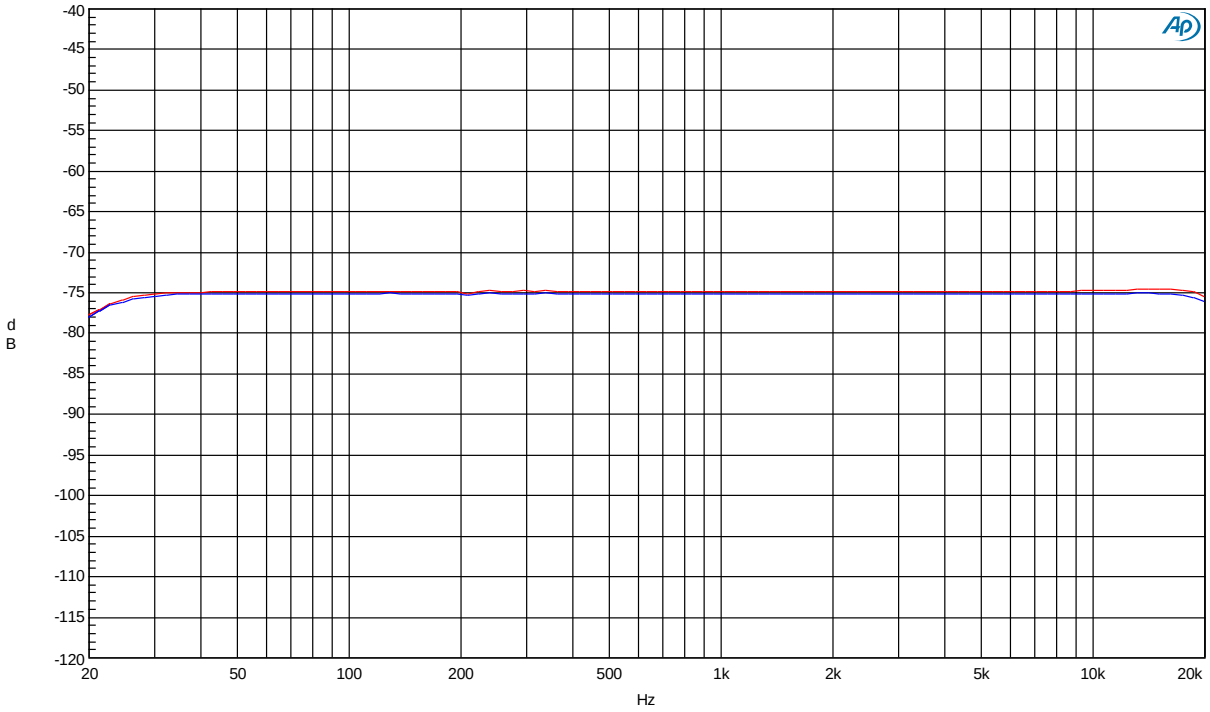


Figure 8. Crosstalk vs. Frequency, Single Ended, 32Ω Load

TYPICAL PERFORMANCE CURVES

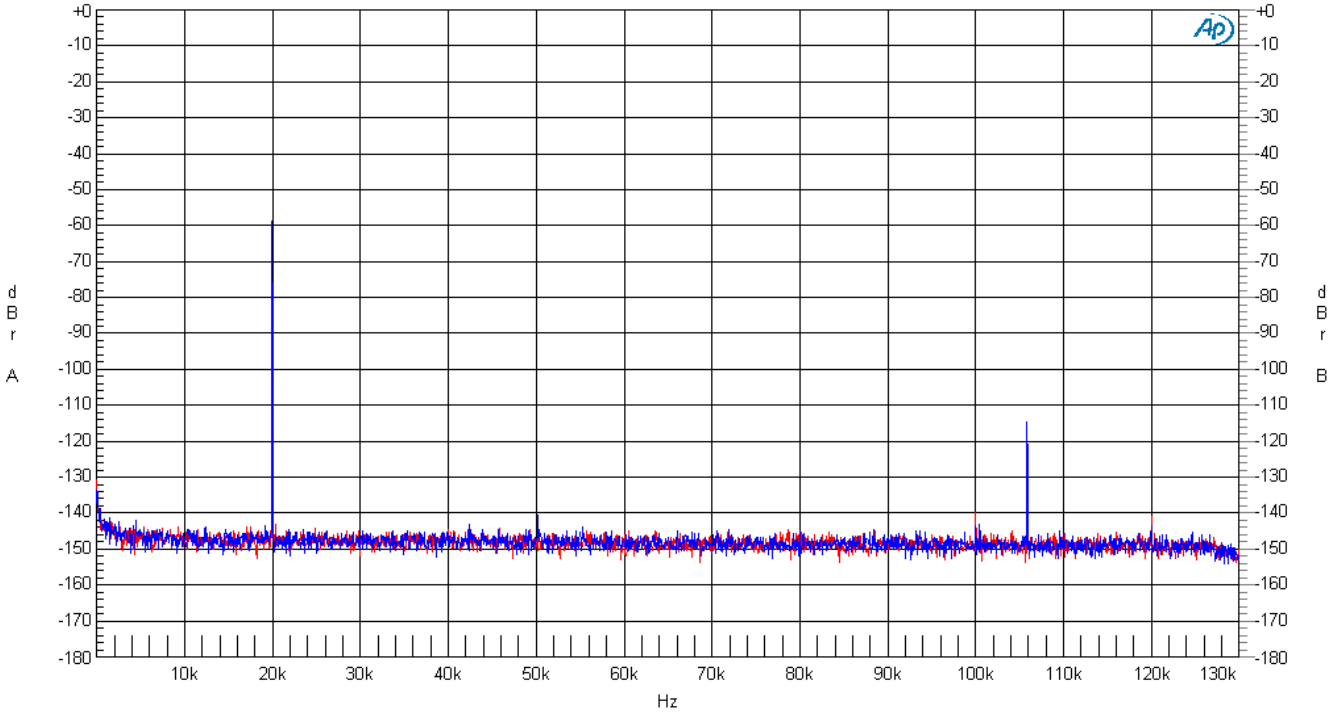


Figure 9. Wideband FFT, 20kHz @ –60dB, Single Ended, 32Ω Load

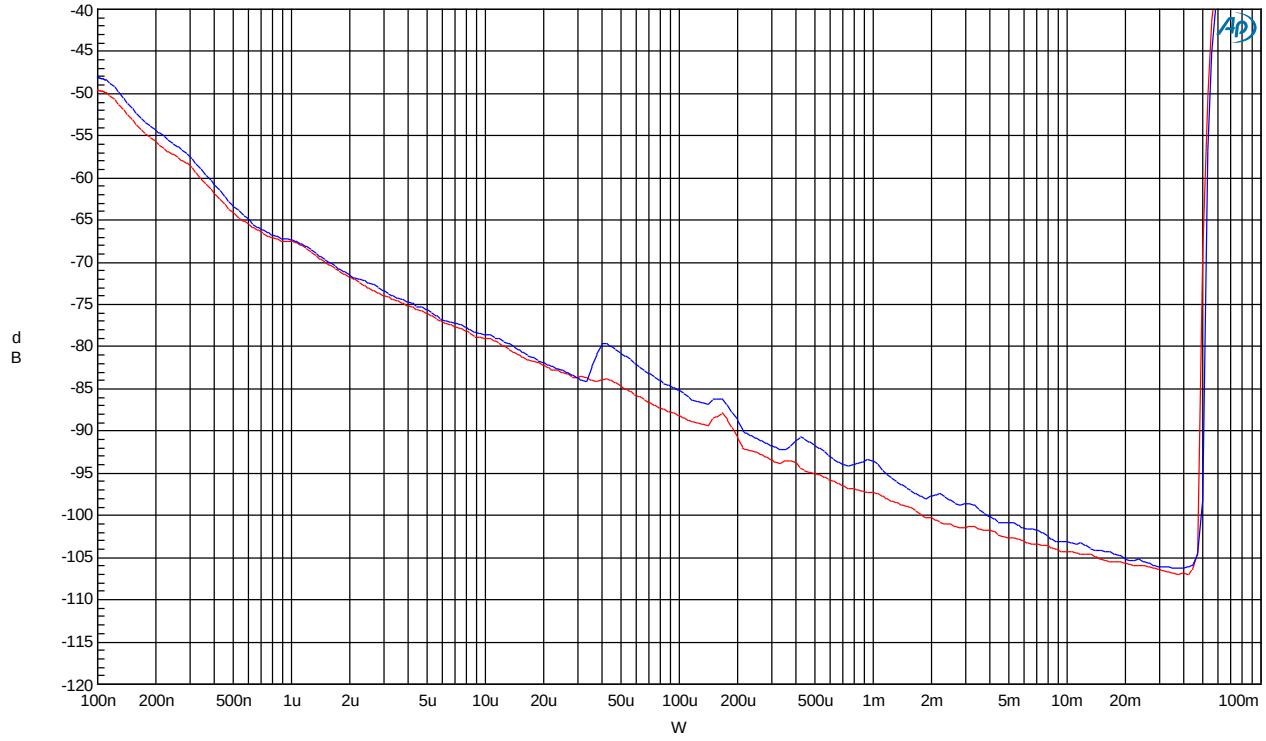


Figure 10. THD+N Unweighted vs. Output Power, Dual Channel Drive, Single Ended, 16Ω Load, external –3.3V supply

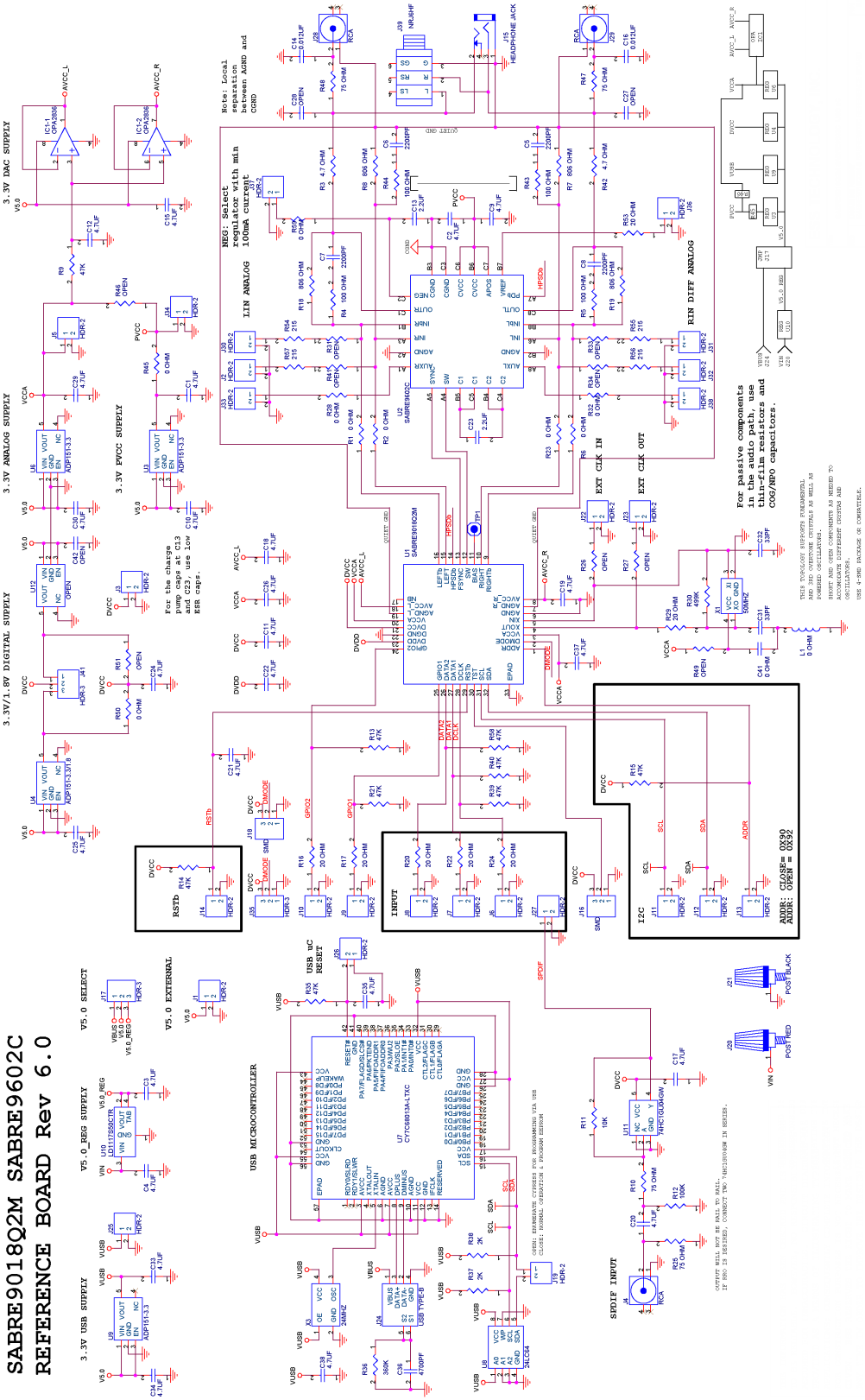
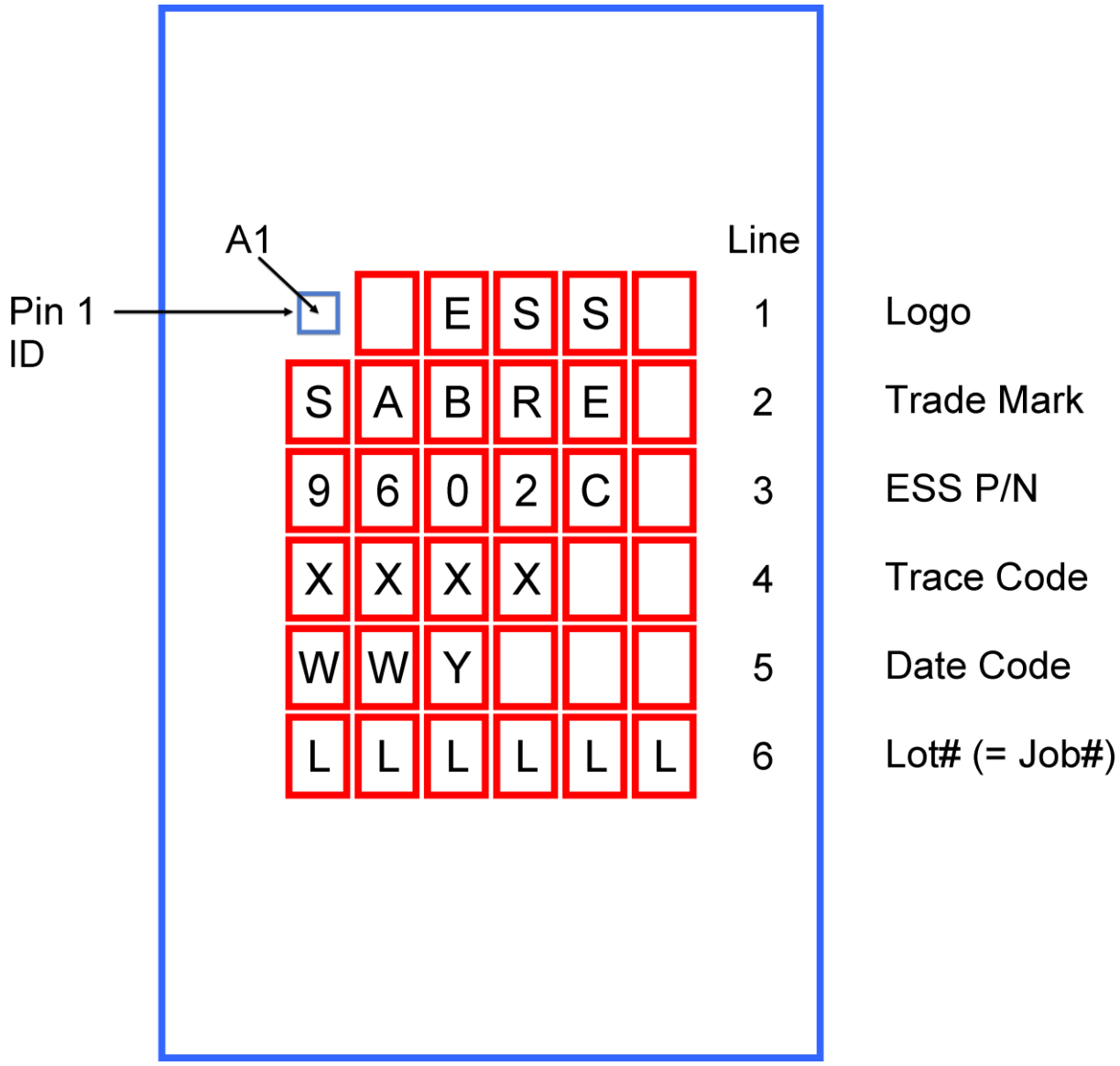


Figure 11. SABRE9602C Reference Design

24-Ball CSP Top View Marking

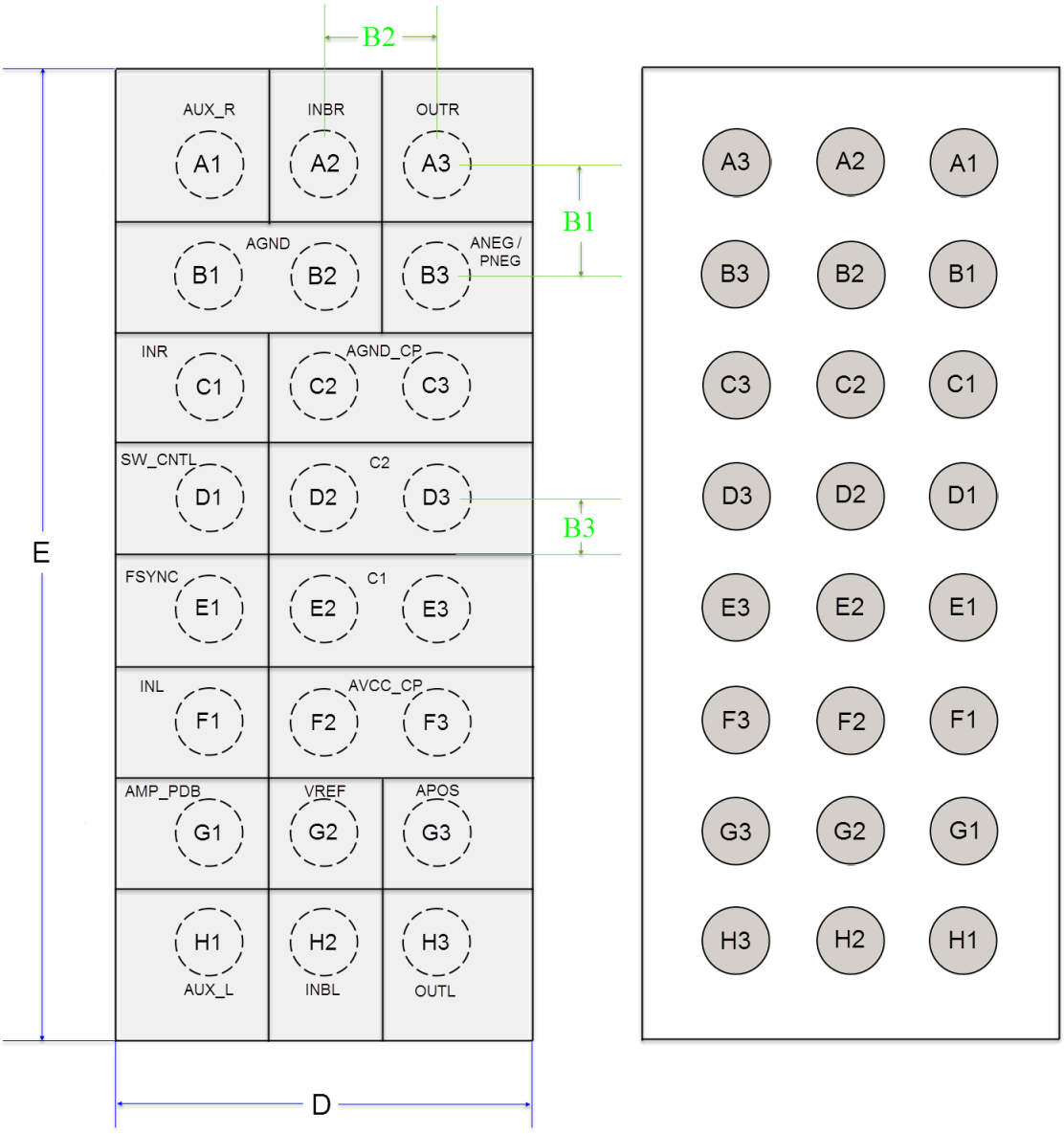


GENERAL MARKING CRITERIA

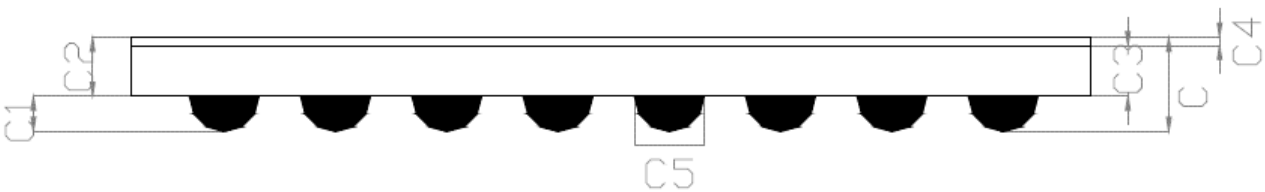
1. Marking to be centered on package
2. Line 1 to be center justified
3. Lines 2 to 6 to be left hand justified
4. Square Dot (ball A1 location) is at the top left corner
5. Font type: ARIAL
6. Laser-mark

Line No.	Character Space	Space Contents
Line 1:	2 thru 4	**ESS**
Line 2:	1 thru 5	**SABRE**
Line 3:	1 thru 5	**9602C**
Line 4:	1 thru 4	First 4 letters of the Trace Code
Line 5:	1 thru 3	Date Code WWY (WW = workweek, Y = year: ’14 = 4, ’15 = 5, ’16 = 6)
Line 6:	1 thru 6	5th to 10th characters of the ESS Lot number.
Backside:		

24-Ball CSP Mechanical Dimensions



Top-Through View (Bumps Down) **Bottom View (Bumps Up)**



Side View

24-Ball CSP Mechanical Dimensions

	Callouts		Normal	Min	Max
	View	Symbol	Millimeters		
Package Body Dimension D	Top View	D	1.450	1.420	1.480
Package Body Dimension E	Top View	E	3.460	3.430	3.490
Backside mark to edge distance D	Top View	Z1	0.200	0.100	0.300
Backside mark to edge distance E	Top View	Z2	1.000	0.900	1.100
Package Height	Side View	C	0.450	0.400	0.500
Ball Height	Side View	C1	0.130	0.100	0.160
Package Body Thickness	Side View	C2	0.320	0.300	0.340
Si Thickness	Side View	C3	0.310	0.295	0.325
Back side coating	Side View	C4	0.010	0.005	0.015
Ball Dimension	Side View	C5	0.200	0.170	0.230
Ball Pitch E	BGA View	B1	0.400		
Ball Pitch D	BGA View	B2	0.400		
Ball Center to Chip Center X	BGA View	B3	0.200		
Total Ball Count	BGA View	N	24		

Table 1. Package Dimensions

Ball Matrix	A	B	C	D	E	F	G	H
1	AUX_R	AGND	INR	SW_CNTL	FSYNC	INL	AMP_PDB	AUX_L
2	INBR	AGND	AGND_CP	C2	C1	AVCC_CP	VREF	INBL
3	OUTR	ANEG/PNEG	AGND_CP	C2	C1	AVCC_CP	APOS	OUTL

Table 2. Ball Matrix

Notch Orientation	Up	Down	Right	Left	Other
		X			

Table 3. Package Orientation

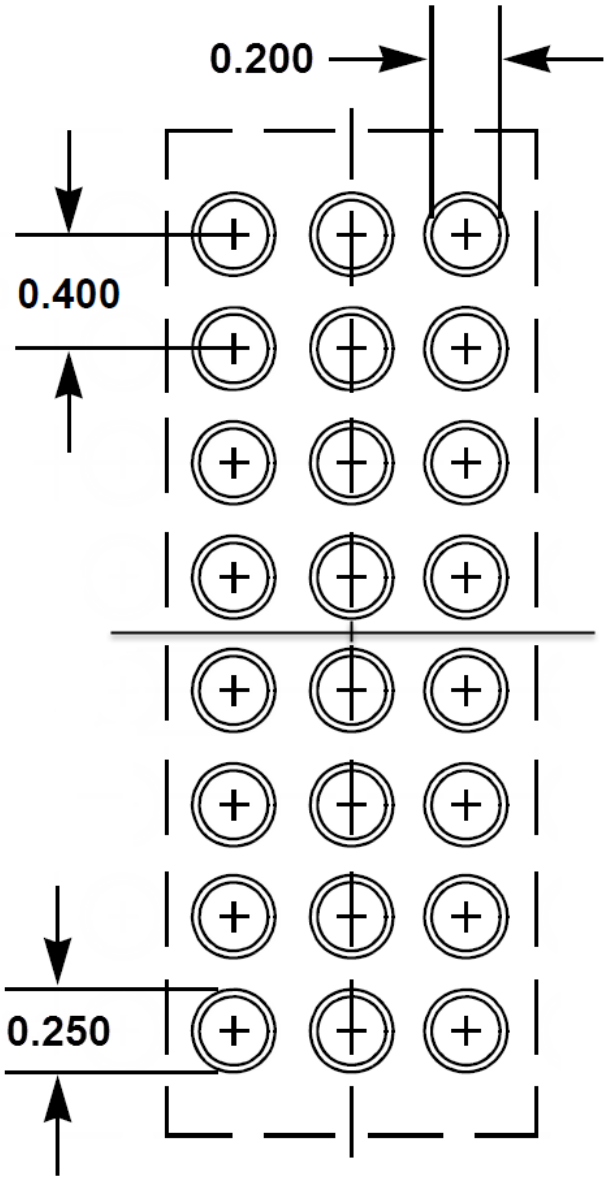
24-Ball CSP Mechanical Dimensions

Position	Ball Name	D	E
A1	AUX_R	400	–1400
A2	INBR	0	–1400
A3	OUTR	–400	–1400
B1	AGND	400	–1000
B2	AGND	0	–1000
B3	ANEG & PNEG	–400	–1000
C1	INR	400	–600
C2	AGND_CP	0	–600
C3	AGND_CP	–400	–600
D1	SW_CNTL	400	–200
D2	C2	0	–200
D3	C2	–400	–200
E1	FSYNC	400	200
E2	C1	0	200
E3	C1	–400	200
F1	INL	400	600
F2	AVCC_CP	0	600
F3	AVCC_CP	–400	600
G1	AMP_PDB	400	1000
G2	VREF	0	1000
G3	APOS	–400	1000
H1	AUX_L	400	1400
H2	INBL	0	1400
H3	OUTL	–400	1400

Ball center coordinates are measured from the BGA VIEW center (0,0)

Table 4. Ball Positioning

Example 24-Ball CSP Land Pattern



Notes:

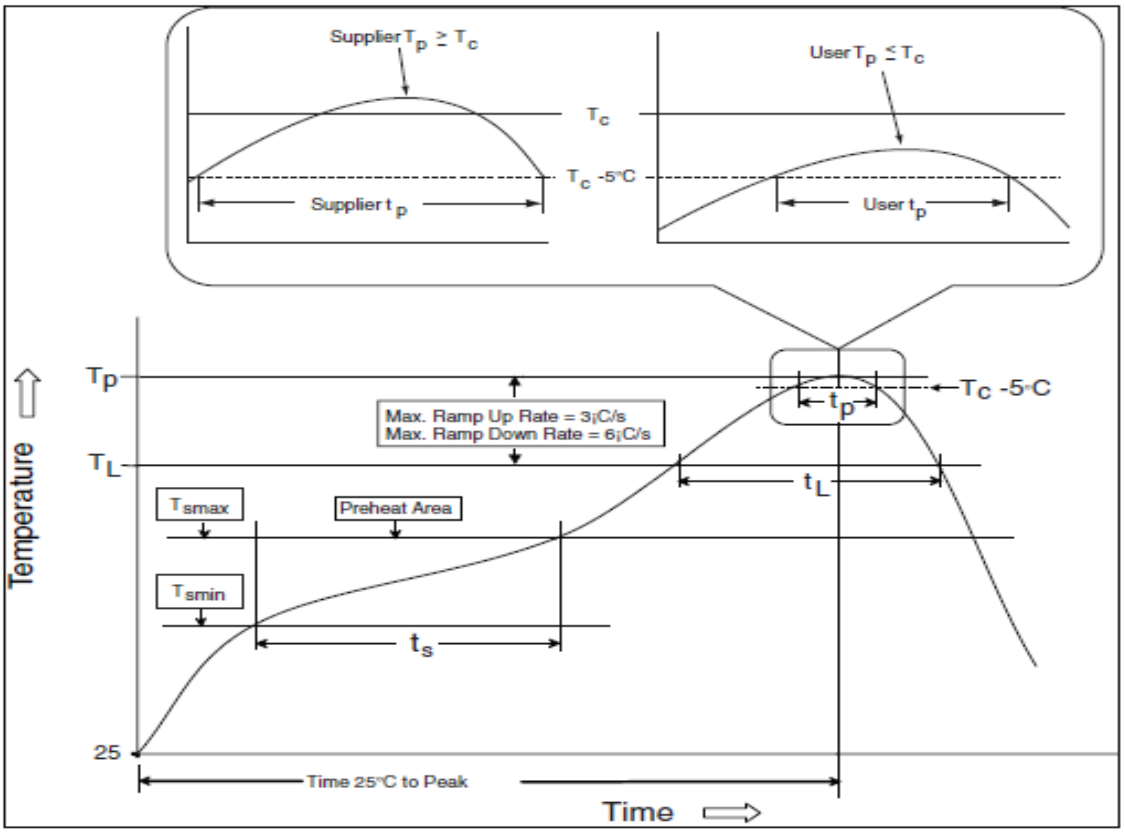
1. All dimensions are in millimeters unless specified otherwise.
2. Thermal vias should be 0.3mm to 0.33mm in diameter, with the barrel plated to 1oz copper.
3. For maximum solder mask in the corners, round the inner corners of each row.
4. For applications where solder loss through vias is a concern, plugging or tenting of the vias should be used. The solder mask diameter for each via should be 0.1mm larger than the via diameter.

Reflow Process Considerations

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor you need to consider.
The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size *(Table RPC-2)*. This narrows the process window for lead-free soldering to 10°C to 20°C.
The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.
Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits *(Table RPC-2)*.

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

Figure RPC-1. IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)



Note: Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual Soldering:
Allowed up to 2 times with maximum temperature of 350 degrees no longer than 3 seconds.

Table RPC-1 Classification reflow profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second max.
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc), see Figure RPC-1	30* seconds
Ramp-down rate (Tp to TL)	6°C / second max.
Time 25°C to peak temperature	8 minutes max.
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp **shall** be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile **shall** be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.
For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

Note 3: All components in the test load **shall** meet the classification profile requirements.

Table RPC-2 Pb-Free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Note 1: At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or non-integral heat sinks.

Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

ORDERING INFORMATION

Part Number	Description	Package
SABRE9602C	Sabre Headphone Driver with Output Switch	24-ball CSP

The letter C identifies the package type CSP.

Revision History

Rev.	Date	Notes
0.1	September 10, 2014	Initial release
0.2	September 18, 2014	Updated block diagram, Figure 1. Added V_{OS} & I_B specifications
0.3	November 10, 2014	Updated cover page specifications and application circuit. Added specifications under Analog Performance.
0.4	November 20, 2014	Corrected error in maximum output power ratings.
0.5	December 4, 2014	Updated DNR and THD+N specifications.
0.6	December 12, 2014	Updated quiescent current and shutdown current specifications.
0.7	December 18, 2014	Added THD specification. Updated Block Diagram and Application Diagram.
0.8	January 28, 2015	Added typical performance graphs.
0.9	February 20, 2015	Added maximum input voltage specification for the Auxiliary Inputs.
1.0	April 28, 2015	Added information on switching to the AUX inputs with SW_CNTL. Updated ESS' contact information.
1.1	June 15, 2015	Standby current changed from 300μA to < 5μA. Added top view showing ball locations and functions.
1.2	July 24, 2015	SABRE9602 block diagram simplified. Added detailed description of product marking plus diagram
1.3	August 19, 2015	Corrected package dimensions in Table 1
1.4	September 16, 2015	Updated CSP Marking diagram and marking criteria. Corrected CSP example land pattern dimensions. Added Charge Device Model ESD rating
1.5	March 14, 2016	Added recommended frequency range for FSYNC when an external oscillator is used

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